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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/060,661	01/30/2002	Zhigang Hu	Hu 1-8-1	6728

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EXAMINER	
WANG, ALBERT C	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 07/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/060,661	HU ET AL.	
	Examiner	Art Unit	
	Albert Wang	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *June 6, 2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Original claims 1-28 are pending.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claim 1 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 09/865,847. An obviousness-type double type patenting rejection is appropriate where the conflicting claims are not identical, but an examined application claim is not patentably distinct from the reference claim(s) because the examined claim is either anticipated by, or would have been obvious over, the reference claim(s). See e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985). Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 1 is generic to the cache memory recited in claim 1 of the copending application. That is, claim 1 of the copending application falls entirely within the scope of claim 1, or, in other words, claim 1 is anticipated by claim 1 of the copending application. Specifically, since a single timer is a subset of a plurality of timers,

the cache memory of claim 1 reciting "a timer associated with at least one of said plurality of caches lines" is anticipated by claim 1 of the copending application reciting "a timer associated with each of said plurality of caches lines".

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-6, 9, 12-17, 20 and 23-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Stefanos Kaxiras, Zhigang Hu, Girija Narlikar, Rae McLellan, *Cache-Line Decay: A Mechanism to Reduce Cache Leakage Power*, First International Workshop on Power-Aware Computer Systems (PACS 2000), pp. 82-96, November 12, 2000 (hereinafter "Kaxiras").

As per claim 1, Kaxiras discloses a cache memory, comprising:

a plurality of cache lines for storing a value from main memory, at least one of said cache lines having an associated cache line decay interval (sec. 2, paragraph 3); and

a timer associated with at least one of said plurality of cache lines, at least one of said timers configured to control a signal that removes power to said associated cache line after said cache line decay interval (sec. 2.1; paragraph 1; fig. 2).

As per claim 2, Kaxiras discloses a timer associated with a given cache line is reset each time said associated cache line is accessed (sec. 2.1; paragraph 1).

As per claim 3, Kaxiras discloses said cache line decay interval is adjusted based on a performance evaluation of said cache memory (sec. 5, paragraph 2).

As per claim 4, while Kaxiras discloses adjusting the cache line decay interval (sec. 5, paragraph 2), Kaxiras is silent with respect to increasing said cache line decay interval following a cache miss for said associated cache line. Such an optimizing step is implied in view of the experimental results (sec. 4.1; fig. 6), which show that miss rate can be significantly decreased when the decay interval is increased from 1K to 8K.

As per claim 5, while Kaxiras discloses adjusting the cache line decay interval (sec. 5, paragraph 2), Kaxiras is silent with respect to decreasing said cache line decay interval following a successful cache decay. Such an optimizing step is implied in view of the experimental results (sec. 4.1; fig. 6), which show that the active ratio (related to power consumption) is significantly decreased with only slight increase in miss rate when the decay interval is decreased from 512K to 64K.

As per claim 6, Kaxiras discloses said decay interval adjustment is implemented by adjusting a reference value in a comparator (sec. 2.1, Global counter).

As per claim 9, Kaxiras discloses said timer is a k bit timer and said timer receives a tick from a global N-bit counter where k is less than N (sec. 2.1, paragraph 2; fig. 2).

As per claim 12, Kaxiras discloses said removing power from said associated cache line resets a valid field associated with said cache line (figs 2 & 4, valid bit; sec. 2.1, Implementation details).

As per claim 13, Kaxiras discloses said timer is an analog device that detects a predefined voltage on said device corresponding to said decay interval (sec. 2.2).

As per claim 14, Kaxiras discloses a method for reducing leakage power in a cache memory, said cache memory having a plurality of cache lines, said method comprising the steps of:

resetting a timer each time a corresponding cache line is accessed (sec. 2.1; paragraph 1);

removing power from said associated cache line after said timer reaches a cache line decay interval (sec. 2, paragraph 3; sec. 2.1; paragraph 1); and

adjusting said cache line decay interval for at least one of said cache lines based on an evaluation of a performance of said cache memory (sec. 5, paragraph 2).

As per claim 15, while Kaxiras discloses adjusting the cache line decay interval (sec. 5, paragraph 2), Kaxiras is silent with respect to increasing said cache line decay interval following a cache miss for said associated cache line. Such an optimizing step is implied in view of the experimental results (sec. 4.1; fig. 6), which show that miss rate can be significantly decreased when the decay interval is increased from 1K to 8K.

As per claim 16, while Kaxiras discloses adjusting the cache line decay interval (sec. 5, paragraph 2), Kaxiras is silent with respect to decreasing said cache line decay interval following a successful cache decay. Such an optimizing step is implied in view of the experimental results (sec. 4.1; fig. 6), which show that the active ratio (related to power consumption) is significantly decreased with only slight increase in miss rate when the decay interval is decreased from 512K to 64K.

As per claim 17, Kaxiras discloses said step of adjusting said cache line decay interval is implemented by adjusting a reference value in a comparator (sec. 2.1, Global counter).

As per claim 20, Kaxiras discloses said timer is a k bit timer and said timer receives a tick from a global N-bit counter where k is less than N (sec. 2.1, paragraph 2; fig. 2).

As per claim 23, Kaxiras discloses said removing power from said associated cache line resets a valid field associated with said cache line (figs 2 & 4, valid bit; sec. 2.1, Implementation details).

As per claim 24, Kaxiras discloses said timer is an analog device that detects a predefined voltage on said device corresponding to said decay interval (sec. 2.2).

As per claim 25, Kaxiras discloses an integrated circuit, comprising:

a cache memory having a plurality of cache lines for storing a value from main memory, at least one of said cache lines having an associated cache line decay interval (sec. 2, paragraph 3); and

a timer associated with at least one of said plurality of cache lines, at least one of said timers configured to control a signal that removes power to said associated cache line after said cache line decay interval (sec. 2.1; paragraph 1; fig. 2).

As per claim 26, Kaxiras discloses said cache line decay interval is adjusted based on a performance evaluation of said cache memory (sec. 5, paragraph 2).

As per claim 27, while Kaxiras discloses adjusting the cache line decay interval (sec. 5, paragraph 2), Kaxiras is silent with respect to increasing said cache line decay interval following a cache miss for said associated cache line. Such an optimizing step is implied in view of the experimental results (sec. 4.1; fig. 6), which show that miss rate can be significantly decreased when the decay interval is increased from 1K to 8K.

As per claim 28, while Kaxiras discloses adjusting the cache line decay interval (sec. 5, paragraph 2), Kaxiras is silent with respect to decreasing said cache line decay interval following a successful cache decay. Such an optimizing step is implied in view of the experimental results (sec. 4.1; fig. 6), which show that the active ratio (related to power consumption) is significantly decreased with only slight increase in miss rate when the decay interval is decreased from 512K to 64K.

4. Claims 11 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaxiras as applied to claims 1 and 14 above, and further in view of Fuller, U.S. Patent No. 5,632,038.

As per claims 11 and 22, Kaxiras does not expressly teach a dirty bit associated with at least one of said cache lines. Fuller teaches a dirty bit associated with at least one of said cache lines to indicate when a contents of said cache line must be written back to main memory before said power is removed from said associated cache line (col. 7, lines 28-38). At the time of the invention, it would have been obvious to one skilled in the art to apply Fuller's dirty bit to Kaxiras' cache memory. A motivation for doing would have been to indicate when to back up data before removing power to cache memory.

5. Claims 7, 8, 10, 18, 19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaxiras as applied to claims 1 and 14 above, and further in view of Philips Semiconductors Datasheet, "74HC/HCT9323A Programmable ripple counter with oscillator", October 27, 1995 (hereinafter "Philips").

As per claims 7 and 18, Kaxiras does not expressly teach said decay interval adjustment is implemented by varying the number of active bits in a local counter. Philips teaches a programmable counter in which the number of active bits may be varied (page 3, inputs S1 & S2 select mode of 3-stage counter). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Philips's programmable counter as the local counter in Kaxiras' cache memory. A motivation for doing so would have been to increase flexibility by introducing another parameter for adjusting the decay interval.

As per claims 8 and 19, any one of a number of external global counters may selected to be input into Philips programmable counter (page 3, via clock input X1).

As per claims 18 and 21, any one of a number of external global counters may selected to be input into Philips programmable counter (page 3, via clock input X1).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 571-272-3669. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

aw
June 24, 2005

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